WHAT IS CLAIMED IS:

1 A quantum computing device, comprising:

a quantum bit structure coupling a quantum box electrode and a counter electrode by sandwiching a first tunnel barrier;

a first gate electrode coupling with the quantum box electrode through a static capacitance;

a trap electrode coupling with the quantum box electrode through a second tunnel barrier; and

a single electron transistor,

wherein the single electron transistor, further comprising a source electrode, drain electrode, an island electrode, and a second gate electrode coupling with the island electrode,

wherein the trap electrode and the island electrode of the single electron transistor being coupled through a readout capacitance.

2 A quantum computing device according to claim 1, wherein the quantum box electrode, the counter electrode, and the trap electrode are composed of a superconducting material.

3 A quantum computing device according to claim 1, wherein a carrier relaxation time through the second tunnel barrier is longer than a coherent vibration period through the first tunnel barrier.

4 A quantum computing device according to claim 3, wherein the carrier relaxation time through the second tunnel barrier is between 5 times to 1000

times of the coherent vibration period through the first tunnel barrier.

5 A quantum computing device according to claim 1, wherein the first tunnel barrier is consist of a first insulating film and the second tunnel barrier is consist of a second insulating film, wherein a thickness of the second insulating film being thicker than a thickness of the first insulating film.

6 A quantum computing device according to claim 5, wherein the thickness of the second insulating film is between 1 times to 3 times of the thickness of the first insulating film.

7 A quantum computing device according to claim 1, wherein the island electrode is coupled with the source electrode through a third tunnel barrier, and coupled with the drain electrode through a fourth tunnel barrier.

8 A quantum computing device according to claim 1, wherein the quantum computing device is configured such that, by applying a negative bias voltage to the counter electrode, thereby extracting an excess Cooper-pair existing in the superconducting box electrode to the trap electrode when the negative bias is applied and accumulating the excess Cooper-pair in the trap electrode, a change of current value flowing in the single electron transistor before and after the extraction of the excess Cooper-pair is measured.

9 A quantum computing device according to claim 1, wherein the quantum computing device is configured such that, by applying a positive bias voltage to the trap electrode, thereby extracting an excess Cooper-pair existing in the

superconducting box electrode to the trap electrode when the positive bias is applied and accumulating the excess Cooper-pair in the trap electrode, a change of current value flowing in the single electron transistor before and after the extraction of the excess Cooper-pair is measured.

10 A quantum bit readout processing unit of a quantum computing device, comprising:

a single electron transistor comprising a source electrode, a drain electrode, an island electrode, and a gate electrode coupling with the island electrode through a gate capacitance; and

a trap electrode coupling with the island electrode through a readout capacitance as well as coupling with a quantum box electrode of the quantum computing device through a tunnel barrier,

wherein the quantum bit readout processing unit being configured so that a change of current value flowing in the single electron transistor is measured before and after extraction of an excess Cooper-pair existing in the quantum box electrode to the trap electrode when a bias voltage is applied to the quantum computing device.

11 A quantum bit readout processing unit of a quantum computing device according to claim 10, wherein the quantum computing device, comprising:

a quantum bit structure coupling the quantum box electrode and a counter electrode through a first tunnel barrier;

a gate electrode coupling with the quantum box electrode through a static capacitance; and

the trap electrode coupling with the quantum box electrode through a

second tunnel barrier.

12 A quantum bit readout processing unit of a quantum computing device according to claim 11, wherein the bias voltage to be applied to the quantum computing device is a negatively biased voltage which is applied to the counter electrode.

13 A quantum bit readout processing unit of a quantum computing device according to claim 11, wherein the bias voltage applied to the quantum computing device is a positively biased voltage applied to the trap electrode.

14 A quantum bit readout processing unit of a quantum computing device according to claim 11, wherein the quantum box electrode, the counter electrode, and the trap electrode are composed of a superconducting material.

15 A quantum bit readout processing unit of a quantum computing device according to claim 11, wherein a carrier relaxation time through the second tunnel barrier is longer than a coherent vibration period through the first tunnel barrier.

16 A quantum bit readout processing unit of a quantum computing device according to claim 15, wherein the carrier relaxation time through the second tunnel barrier is between 5 times to 1000 times of the coherent vibration period through the first tunnel barrier.

17 A quantum bit readout processing unit of a quantum computing device according to claim 11, wherein the first tunnel barrier is consist of a first insulating film and the second tunnel barrier is consist of a second insulating film, wherein a thickness of the second insulating film being thicker than a thickness of the first insulating film.

18 A quantum bit readout processing unit of a quantum computing device according to claim 17, wherein the thickness of the second insulating film is between 1 times to 3 times of the thickness of the first insulating film.

19 A quantum bit readout processing unit of a quantum computing device according to claim 10, wherein the island electrode is coupled with the source electrode through a third tunnel barrier, and coupled with the drain electrode through a fourth tunnel barrier.

20 A quantum bit readout method of a quantum computing device, comprising steps of:

extracting an excess Cooper-pair existing in a quantum box electrode to a trap electrode of a quantum computing device when a bias voltage is applied to the quantum computing device; and

measuring a change of a current value flowing in a single electron transistor, which includes an island electrode coupling with the trap electrode through a readout capacitance, before and after the extracting of the excess Cooper-pair.

21 A quantum bit readout method of a quantum computing device according

to claim 20, wherein the bias voltage applied to the quantum computing device is a negatively biased voltage applied to a counter electrode of the quantum computing device.

22 A quantum bit readout method of a quantum computing device according to claim 20, wherein the bias voltage to be applied to the quantum computing device is a positively biased voltage which is applied to the trap electrode.